Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845 Chipset Platform for DDR

Design Guide Update

March 2004

Notice: The Intel® 845 chipset family may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the Specification Update.

Document Number: 298595-003

Content

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release	April 2002
-002	(1) Added Documentation Change #3, Change Table 3, System Bus Routing Summary for the Processor (2) Added Documentation Change #4, Add Section 13.2, Intel® Boxed Processor Mechanical Keep-Outs (3) Added Documentation Change #5, Add Section 15.1.3, Intel® Boxed Processor Mechanical Keep-Outs	May 2002
-003	(1) Added Documentation Change #6, Revision –Intel® ICH2 Schematic Checklist	March 2004

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Preface

This Design Guide Update document is an update to the specifications and information contained in the *Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845 Chipset Platform for DDR Design Guide*, February 2002. This Design Guide Update may reference other documents listed in the following Affected Documents/Related Documents table. This document is a compilation of updates to the general design considerations; schematic, layout, and routing updates; and documentation changes. This document is intended for hardware system manufacturers and for software developers of applications, operating systems, and tools. The design guide (and this design guide update) is primarily targeted at the PC market segment and was first published in 2002. Those using this design guide and update should check for device availability before designing in any of the components included in this document.

Information types defined in the Nomenclature section of this document are consolidated into the public design guide update document when the public design guide document is first published. This design guide update document contains a complete list of all known information types.

Affected Documents

Document Title	Document Number
Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845 Chipset Platform for DDR Design Guide, February 2002	298605-002

Related Documents

Document Title	Document Number
Intel® 845 Chipset: 82845 Memory Controller Hub (MCH) for DDR Datasheet, January 2002	298604-001
Intel® 82801BA (ICH2) I/O Controller Hub Datasheet	290687-002

Nomenclature

General Design Considerations include system level considerations that the system designer should account for when developing hardware or software products using the Intel® 845 Chipset: 82845 Memory Controller Hub (MCH) for DDR.

Schematic, Layout, and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Codes Used in Summary Table

Doc:	Document change or update that will be implemented.
Shaded:	This item is either new or modified from the previous version of the document.

NO.	Plans	GENERAL DESIGN CONSIDERATIONS
		There are no General Design Consideration changes in this Design Guide Update revision.

NO.	Plans	SCHEMATIC, LAYOUT, AND ROUTING UPDATES
		There are no Schematic, Layout, and Routing Updates in this Design Guide Update revision.

NO.	Plans	DOCUMENTATION CHANGES
1	Doc	Replace Figure 139, Intel® 845 Chipset Platform Using DDR System Memory Power Delivery Map
2	Doc	Added Section 4.6.7, Electrostatic Discharge Platform Recommendations
3	Doc	Change Table 3, System Bus Routing Summary for the Processor
4	Doc	Add Section 13.2, Intel® Boxed Processor Mechanical Keep-Outs
5	Doc	Add Section 15.1.3, Intel® Boxed Processor Mechanical Keep-Outs
6	Doc	Revise Section 14.1, Schematic Checklist, Host Interface, PWRGOOD

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General Design Considerations

There are no General Design Considerations in this Design Guide Update revision.

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Schematic, Layout, and Routing Updates

There are no Schematic, Layout, and Routing Updates in this Design Guide Update revision.

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Documentation Changes

1. Replaced: Replace Figure 139, Intel® 845 Chipset Platform Using DDR System Memory Power Delivery Map

Figure 139, Intel® 845 Chipset Platform Using DDR System Memory Power Delivery Map, in Section 12.2, has two changes in the ICH2 section:

One ICH2 power plane is added to it. This added ICH2 power plane is “ICH2 V5REF_SUS”. This power plane has always existed in the ICH2. It is not new. This addition to the Power Delivery Map simply shows this ICH2 plane.

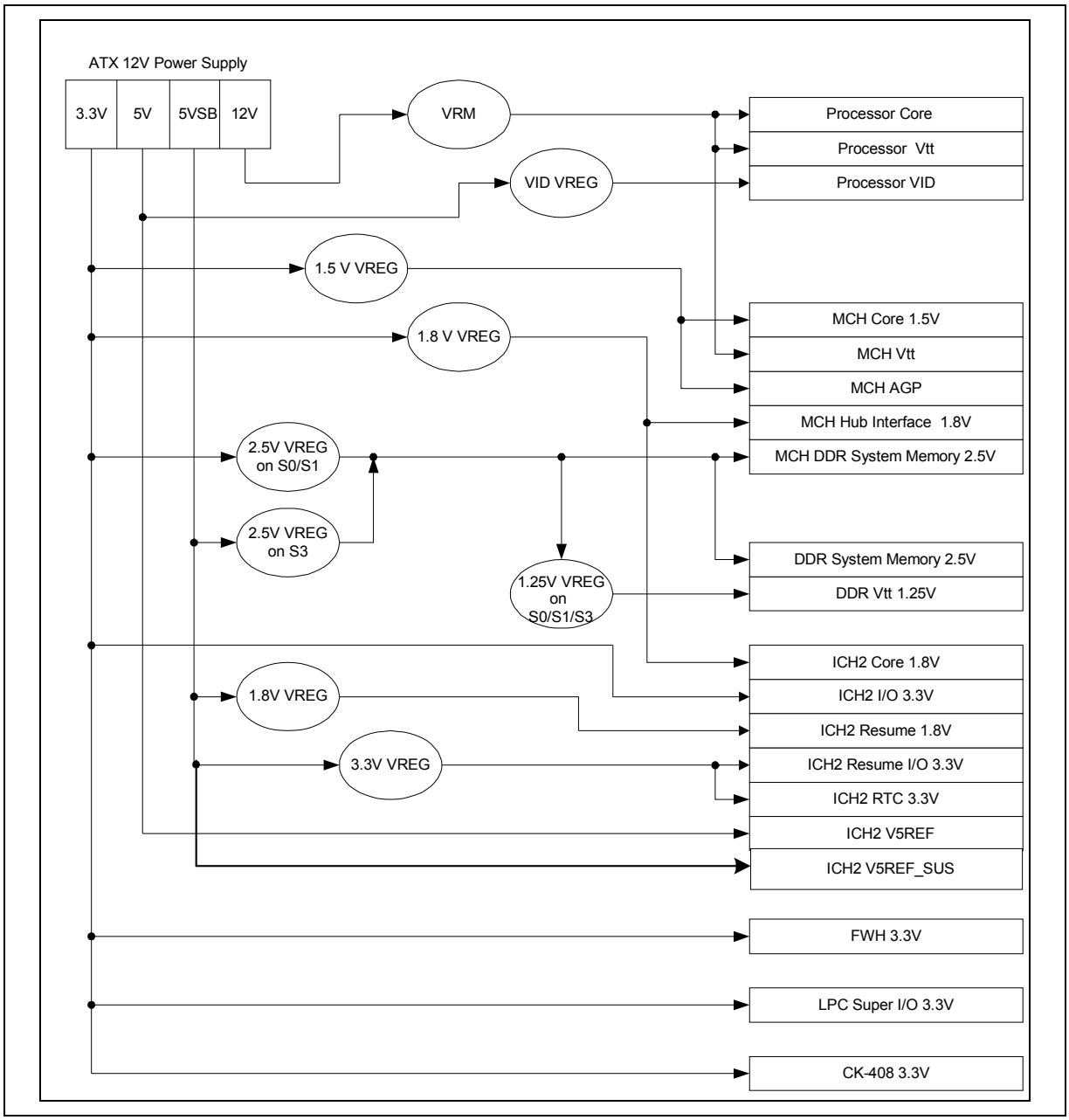
The block labeled “ICH2 5 V” is renamed to “ICH2 V5REF”.

These two changes above also reflect the actual pin names on the ICH2.

A third change is that the two, 2.5 V VREG voltage regulators have corrections to the supported system power states (S0, S1, S2, etc.).

A forth change is that the supported system power states for the 1.25 V VREG voltage regulator have been moved inside the ellipse.

Figure 139 is replaced with the following new Power Delivery Map:


ATX 12V Power Supply
3.3V
5V
5VSB
12V
VRM
VID VREG
1.5 V VREG
1.8 V VREG
2.5V VREG on S0/S1
2.5V VREG on S3
1.25V VREG on S0/S1/S3
1.8V VREG
3.3V VREG
Processor Core
Processor Vtt
Processor VID
MCH Core 1.5V
MCH Vtt
MCH AGP
MCH Hub Interface 1.8V
MCH DDR System Memory 2.5V
DDR System Memory 2.5V
DDR Vtt 1.25V
ICH2 Core 1.8V
ICH2 I/O 3.3V
ICH2 Resume 1.8V
ICH2 Resume I/O 3.3V
ICH2 RTC 3.3V
ICH2 V5REF
ICH2 V5REF_SUS
FWH 3.3V
LPC Super I/O 3.3V
CK-408 3.3V

2. Electrostatic Discharge Platform Recommendations

The following new information is added as Section 4.6.7, *Electrostatic Discharge Platform Recommendations:*

4.6.7 Electrostatic Discharge Platform Recommendations

Electrostatic discharge (ESD) into a system can lead to system instability, and possibly cause functional failures when a system is in use. There are system level design methodologies that when followed can lead to higher ESD immunity. Electromagnetic fields due to ESD are introduced into a system through chassis openings such as the I/O back panel and PCI slots. These fields can introduce noise into signals and cause the system to malfunction. One can reduce the potential for issues at the I/O area by adding more ground plane on the motherboard around the I/O area. This can lead to a higher ESD immunity.

Intel recommends that the I/O area on the top and bottom signal layers of a 4-layer motherboard near the I/O back panel be filled with a ground fill as shown in Figures 1-4. In addition, a ground fill cutout should be placed on the Vcc layer in the area where the ground fill is done on the top and bottom layers. Intel recommends filling the I/O area as much as possible without effecting the signal routing. The board designer should fill the entire I/O area along the board edge.

The spacing from the ground fill to other shapes/traces should be at least 20 mils. It is recommended that these ground fill areas be connected to two chassis mounting holes (as seen in Figure 2). This will allow ESD current to travel to the chassis instead of the board. Ground stitching vias should be placed throughout the entire ground fill if possible. It is important that the vias are placed along the board edge. Ground stitching vias for the ground fill should be 100–150 mils apart or less.

In conclusion, Intel recommends the following:

- Fill the I/O area with the ground fill in all layers including signal layers whenever possible.
- Extend the ground fill along the entire back I/O area.
- Connect the ground fill to mounting holes.
- Place stitching vias 100-150 mils apart in the entire ground fill.

Figure 1. Top Signal Layer before the Ground Fill Near the I/O Area

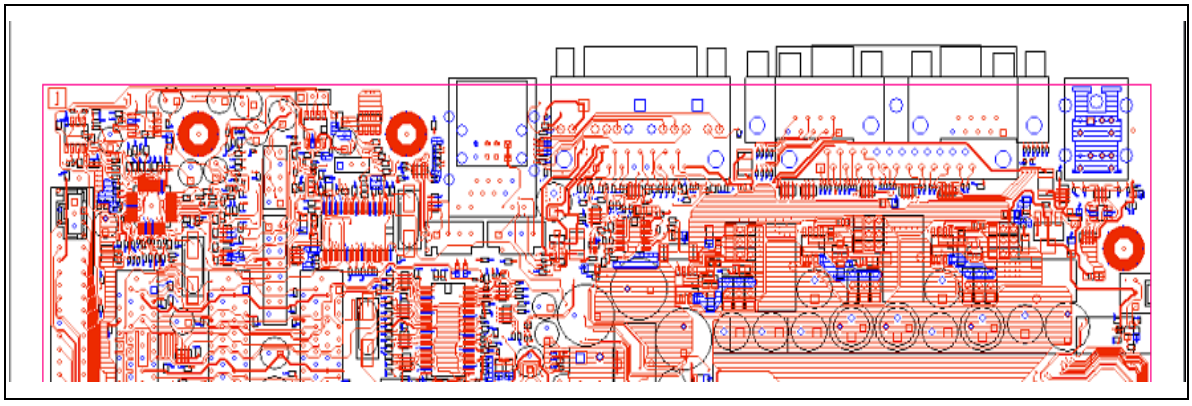


Figure 2. Top Signal Layer after the Ground Fill Near the I/O Layer

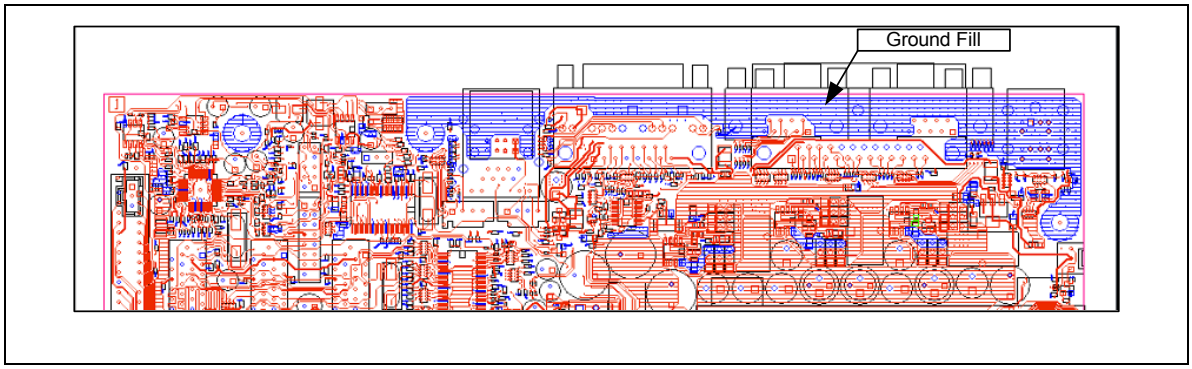


Figure 3. Bottom Signal Layer before the Ground Fill Near the I/O Area

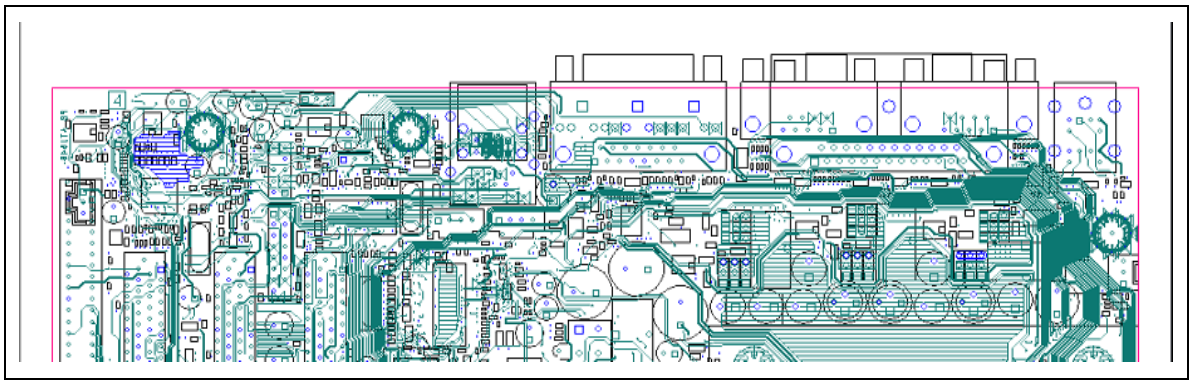
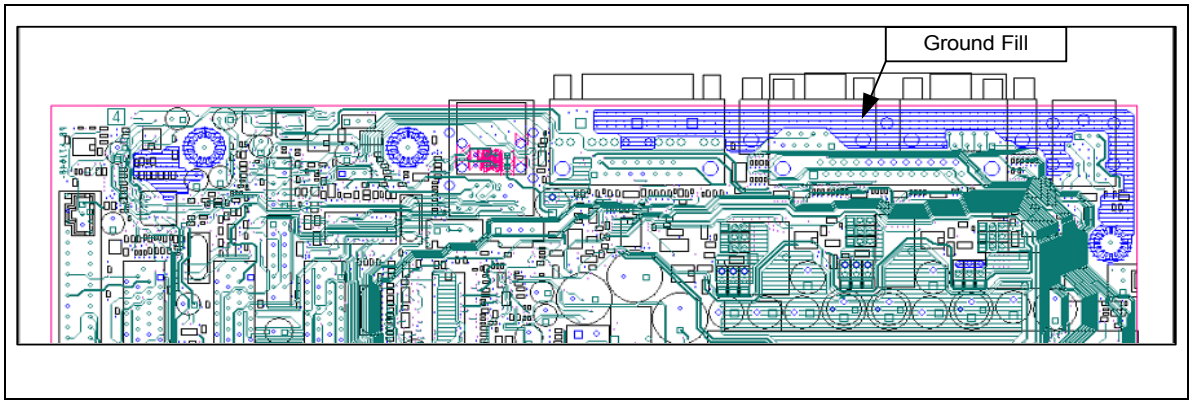


Figure 4. Bottom Signal Layer after the Ground Fill Near the I/O Area



3. Change Table 3, System Bus Routing Summary for the Processor

Reference Table 3, *System Bus Routing Summary for the Processor*, in Section 4.1. The parameter "Clock keep out zones" is changed as shown:

Clock keep out zones	Refer to Table 57, BCLK [1:0]# Routing Guidelines, of this Design Guide

4. Add Section 13.2, Intel® Boxed Processor Mechanical Keep-Outs

The following new section is added:

13.2 Intel® Boxed Processor Mechanical Keep-Outs

Verify Intel's Boxed Processor mechanical keep-outs are marked and visible during board layout. This keep-out zone should be considered during chassis selection.

5. Add Section 15.1.3, Intel® Boxed Processor Mechanical Keep-Outs

The following new section is added:

15.1.3 Intel® Boxed Processor Mechanical Keep-Outs

Checklist Item	
Intel® Boxed Processor Mechanical Keep-Outs	
• Verify Intel's Boxed Processor mechanical keep-outs are marked and visible during board layout. This keep-out zone should be considered during chassis selection.	

6. Revise Section 14.1, Schematic Checklist, Host interface, PWRGOOD

Revise Section 14.1, *Schematic Checklist, Host Interface*, PWRGOOD with the following:

Signal	Description
Processor/Intel® ICH2 Signals	
PWRGOOD	Connects to ICH2 CPUPWRGD pin. Note that a weak pull-up to V_CPU_IO is required and that such value should not exceed the Intel® ICH2's Ioh2/Iol2 specs.

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